PROPAGATION OF MISFIT DISLOCATIONS FROM BUFFER/SI INTERFACE INTO SI

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to U.S. Provisional Patent Application No. 61/091,264,entitled "PROPAGATION OF MISFIT DISLOCATIONS FROM BUFFER/SI INTERFACE INTO SI," which was filed on Aug. 22, 2008 and which is hereby incorporated by reference in its entirety.

STATEMENT OF GOVERNMENTAL SUPPORT

The invention described and claimed herein was made at least in part utilizing funds supplied by AFOSR GRANT No: AFOSRISSAO7NE001 through the U.S. Department of Energy under Contract No. DE-AC02-05CH11231. The Government has certain rights in this invention.

BACKGROUND OF THE INVENTION

Epitaxial growth of GaN on Si substrates has recently gained increased interest since such a system presents possibilities for novel integrated devices based on GaN and Si [1-3] at reduced cost. This is particularly the case for LEDs which are traditionally low cost items and are required in large numbers to meet demand in display and lighting applications. Such a system would provide the potential for utilizing the strength of GaN in conjunction with advanced Si technology and abundance for effective and economical integrated device structures. However, the large misfit between GaN and Si (14% between a-axes), growth of a polar crystal on non-polar substrates and the difference in thermal expansion coefficients lead to a high density of lattice defects and antiphase disorder as observed in GaAs grown on Si [4]. Due to a lack and/or prohibitively high cost of native substrates for growth of GaN, this material needs to be grown on foreign substrates such as Al_2O_3 or SiC. Therefore, different approaches need to be applied, such as lateral overgrowth and pendeo-epitaxy, to reduce defect density in the epi-layer [5-10].

Reduction of strain at the interface leads to a lower defect density. Earlier results [11-12] show that H and He implantation through a pseudomorphic Si—Ge layer grown on (100) Si substrates below critical layer thickness and subsequent annealing at 850° C. leads to complete strain relaxation and defect free Si—Ge layers in comparison with unimplanted samples. The genesis of defect-free growth lies in the fact that implantation energy was chosen to create end of range defects slightly below Si—Ge/Si interface (50-100 nm). The H or He bubbles are formed in Si following annealing. A much denser arrangement of tangled misfit dislocations was found at the interface between the $Si_{1-x}Ge_x$ (x=22% -30%) and Si substrates in comparison with regularly distributed misfit dislocations grown on un-implanted Si, where only 50% relaxation was obtained upon annealing at 1100° C. A model was proposed [11] for strain relaxation due to the formation of dislocation loops in the vicinity of He bubbles that annihilate with threading dislocations at high temperature when the loops become glissile and can glide toward the SiGe interface. It has been proposed that one side of the loop is pinned at the interface where it forms a strain relieving misfit segment. The other side is driven by the mismatch stress to the surface, where an atomic step is generated. In the case of GaN however, pseudomorphic growth on Si is impossible due to the lattice misfit being too large.

Different approaches are therefore needed to permit epitaxial growth of GaN on Si substrates without threading dislocations since pseudomorhic growth of GaN on Si is impossible due to large lattice and thermal expansion mismatch.

SUMMARY OF THE INVENTION

The present invention provides an avenue to reduce defects in GaN (or other III-Nitride based on GaN, such as InGaN or AlGaN) grown on Si as well providing a pathway to adapt GaN technology to mature Si processing technology for improved GaN-based device fabrication. A Si substrate is implanted an ionic species capable upon annealing of forming bubbles stable to the processing conditions of the device fabrication method. In a specific embodiment, He is the implanted species, although others, such as H or Ne, or their combinations with He by multiple implantations, are also possible.

After the implantation, the Si surface is cleaned using conditions that do not cause dissipation of the implanted ions or bubbles formed therefrom to the Si substrate surface. Such a cleaning procedure does not involve a high temperature (e.g., greater than 1000° C.) hydrogen anneal in the growth chamber following a chemical clean to ensure complete removal of any surface oxides prior to epitaxial growth. Cleaning in accordance with the present invention is conducted at a relatively low temperature, below 300° C., for example, about 80° C., or even room temperature. A RCA standard clean process variant, described further below, has been found to be suitable. In accordance with the present invention, such a wet chemical cleaning process, has been found to provide suitable wafer cleaning for high quality epitaxial growth of GaN on Si without the need for a high temperature anneal of the Si substrate in the growth chamber.

A GaN/Si interfacial buffer layer is then grown on the cleaned Si substrate so that a buffer/Si interface is formed. A common GaN/Si interfacial buffer layer material is AlN, although other materials that promote adherence of the GaN to the Si may alternatively be used. The buffer layer growth process is generally a thermal process that also accomplishes annealing of the Si substrate so that bubbles of the implanted ion species are formed in the Si at an appropriate distance from the buffer/Si interface so that the bubbles will not migrate to the Si surface during annealing, but are close enough to the interface so that a strain field around the bubbles will be sensed by dislocations at the buffer/Si interface and dislocations are attracted by the strain field caused by the bubbles and move into the Si substrate instead of into the buffer epi-layer. A layer of AlN followed by GaN (or other III-Nitride based on GaN, such as InGaN or AlGaN) is then grown on the buffer layer.

The growth of the interfacial buffer and GaN (or other III-Nitride based on GaN, such as InGaN or AlGaN) layers can be accomplished by any suitable technique. Molecular Beam Epitaxy (MBE) is a suitable technique for accomplishing the relatively low temperature growth required for the He implantation embodiment of the invention. Metal-Organic Chemical Vapor Deposition (MOCVD) may be a suitable technique where low processing temperatures are not required, such as when Ne is implanted. Another suitable low temperature film growth technique applicable to the present invention is Energetic Neutral Atomic-Beam Lithography/Epitaxy (ENABLE).

In a specific embodiment, He is implanted into the Si substrate with appropriate implant conditions. The implant conditions are selected to guide the implanted ions to concentrate about 100-250 nm, or preferably 120-200 nm, for